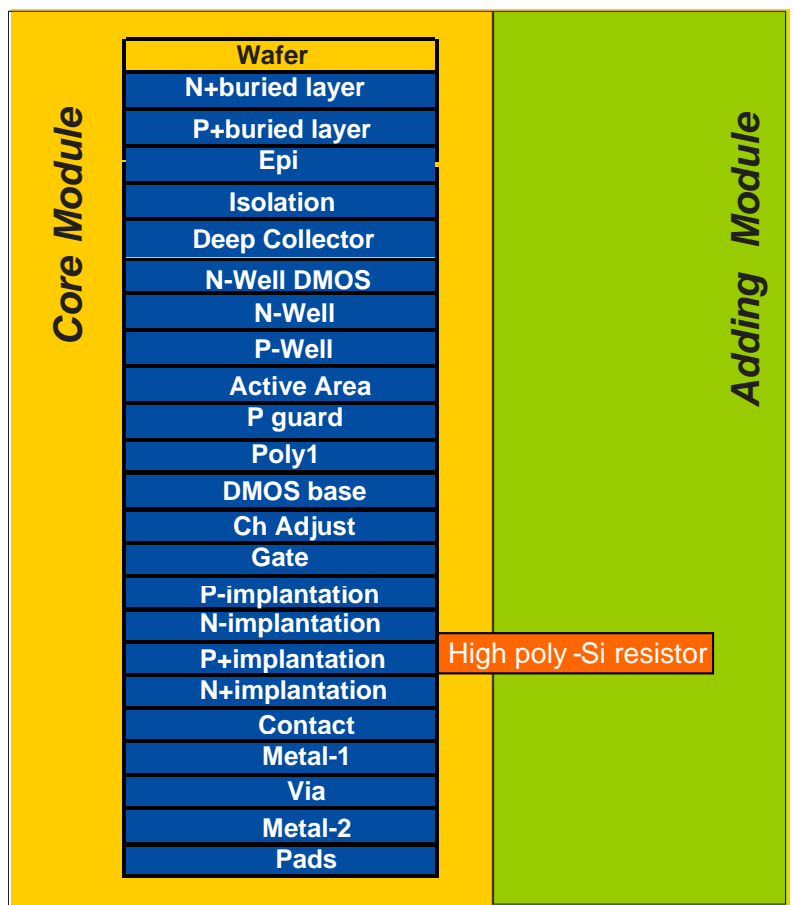




80V BiCDMOS process specification

> Description

- 80V 0.8um BiCDMOS process is DMS Lab Limited BCD smart power technologies. Main target applications are analog switch ICs, driver ICs for capacitive, inductive and resistive loads, automotive driver ICs for applications using not more than 80V absolute maximum supply. The typical breakdown voltage of the DMOS devices more than 80V.
- The modular process combines DMOS and HV CMOS for different supply application with core bipolar, logic CMOS processing steps to provide a wide variety of MOS and bipolar devices with different voltage levels on the same die.
- The 22 layers core process module is available for 80V breakdown voltage of the DMOS. This process module provides locos insulation, double level poly, and two metal levels.
With this core module an optimized n-channel vertical and lateral DMOS transistor, HV CMOS, logic CMOS and some bipolar transistors can be made,
- One more process modules can be added to integrate high value poly-Si resistors and PIP capacitors (1 layer).





> Key Features

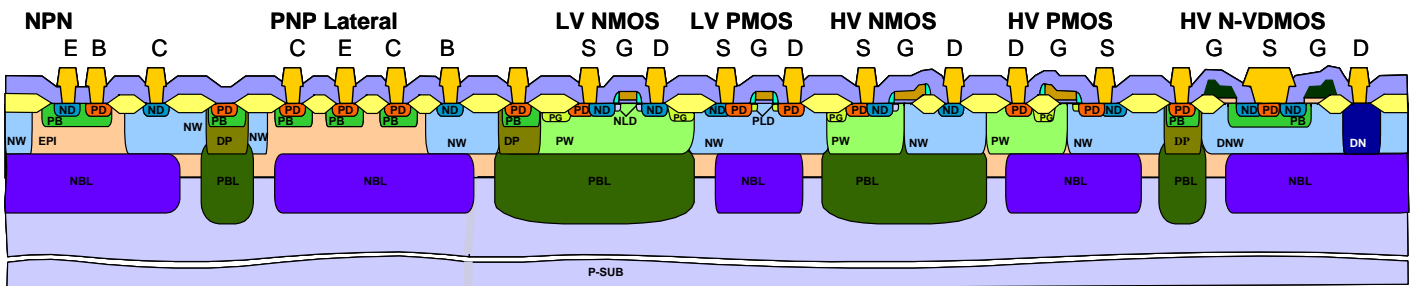
The vertical DMOS transistor with low R_{dson} and small area is the main HV component of the BiCDMOS 80V technology.

0.8um double poly, double metal, triple Well BCD process.

A high number of different devices are available:

- 80V n-channel vertical and lateral DMOS transistor;
- 30V n-channel MOS transistor;
- 30V p-channel MOS transistor;
- 25V n-channel lateral DMOS transistor;
- 10V CMOS transistors;
- Logical 5V CMOS transistors;
- 5V and 30V NPN transistors;
- 5V and 30V PNP transistors;
- Zener diodes and Schottky diodes;
- Gate oxide capacitors;
- Low resistivity poly-Si resistors;
- Resistors in active layers.
 - Optional poly for high value resistor;
 - Optional poly-1 – poly2 capacitors;

> Schematic cross section





> Basic design rules

Layer	Min width (um)	Min spacing (um)
Active Area (CMOS)	2.0	1.5
CMOS Gate	0.8	0.8
DMOS Gate	7.0	--
Contact	0.8	1.0
Metal-1	1.2	1.0
VIA	1.5	1.5
Metal-2	1.5	1.3

> Device Parameters of main elements for 80V process

ELEMENT	PARAMETER	SPEC		MEASUREMENT CONDITIONS
	UNIT	MIN	MAX	
HV NDMOS L=3.5 um, W=100 um	VTH, V	0.5	3.0	Id=0.1uA
	IDS, mA	8.0	-	Ug=Ud=10 V
	BVDS, V	80	-	Id=10uA
	Rsp, mOhm*mm2	-	90	Ug=10 V
	IDS, uA	-	50	Ug=Ub=Us=0 V, Ud =10 V
HV NMOS L=7 um, W=56 um	VTH, V	0.45	0.9	Id=0.1uA
	IDS, mA	0.5	-	Ug=Ud=10 V
	BVDS, V	30	-	Id=10uA
HV PMOS L=6 um, W=56 um	VTH, V	0.7	1.1	Id=0.1uA
	IDS, mA	0.35	-	Ug=Ud=10 V
	BVDS, V	30	-	Id=10uA
LV NMOS L=0.8 um, W=50 um	VTH, V	0.5	0.9	Id=0.1uA
	IDS, mA	15	25	Ug=Ud=5 V
	BVDS, V	10	-	Id=10uA
LV PMOS L=0.8 um, W=50 um	VTH, V	0.7	1.1	Id=0.1uA
	IDS, mA	7.0	12	Ug=Ud=5 V
	BVDS, V	10	-	Id=10uA
HV NPN Se=10x10 um2	BETA	30	100	Ib=10uA, Uc=1 V
	BVCE0, V	30	-	Ic=10uA, floating base
LV NPN Se=10x10 um2	BETA	30	100	Ib=10uA, Uc=1 V
	BVCE0, V	9	-	Ic=10uA, floating base
HV Lateral PNP Wb=15um	BETA	15	-	Ib=-10uA, Uc=-1 V
	BVCE0, V	30	-	Ic=-10uA, floating base
LV Lateral PNP Wb=4um	BETA	15	-	Ib=-10uA, Uc=-1 V
	BVCE0, V	9	-	Ic=-10uA, floating base
Schottky Diode	BV, V	30	-	Id=10uA
Zener Diode	BV, V	7	8	Id=10uA
Base Resistor	RS, Ohm/sq	450	550	Ir=10uA
PolySi- gate oxide – Well capacitor	Ccs, pF/um2	1,7E-3	2.1E-3	F=1MHz, Vmea=5V

Note: () – value for option (adding module)